Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Currently amended): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate ~~conductive layer~~ line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the gate insulating layer separates the pixel electrode from the insulating substrate.

2. (Currently amended): The thin film transistor array panel of claim 1, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo_x or Mo alloy and an upper film of Al or Al alloy.

3. (Currently amended): The thin film transistor array panel of ~~claim 2~~ claim 1, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

4. (Currently amended): The thin film transistor array panel of ~~claim 4~~ claim 1, wherein the pixel electrode comprises IZO.

5. (Currently amended): The thin film transistor array panel of ~~claim 5~~ claim 1, wherein the passivation layer has second and third contact holes exposing end portions of the

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gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

6. (Withdrawn): A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate line on an insulating substrate;

forming a gate insulating layer;

forming a semiconductor layer;

forming a data conductive layer including a data line and a drain electrode;

depositing a passivation layer;

forming a photoresist including a first portion located on an end portion of the gate line, a second portion thicker than the first portion and located on the drain electrode, and a third portion thicker than the second portion;

exposing a portion of the passivation layer under the second portion of the photoresist and a portion of the gate insulating layer under the first portion of the photoresist by etching using the photoresist as an etch mask;

forming first and second contact holes exposing the drain electrode and the end portions of the gate line, respectively; and

forming a pixel electrode connected to the drain electrode through the first contact hole.

7. (Withdrawn): The method of claim 6, wherein the photoresist further comprises a fourth portion disposed on an end portion of the data line, and the method further comprises forming a third contact hole exposing the end portion of the data line.

8. (Withdrawn): The method of claim 6, wherein the exposure is performed by dry etching under a condition that etching ratios for the photoresist and the passivation layer are substantially the same.

9. (Withdrawn): The method of claim 6, wherein the exposed portion of the gate line is thicker than the exposed portion of the passivation layer.

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10. (Withdrawn): The method of claim 6, wherein the formation of the first and second contact holes is performed by dry etching under a condition that etching ratios for the gate insulating layer and the passivation layer are substantially the same.

11. (Withdrawn): The method of claim 6, wherein the gate line or the data line comprises a lower film of Cr, Mo or Mo alloy and an upper film of Al or Al alloy.

12. (Withdrawn): The method of claim 11, further comprising:

removing the upper film before forming the pixel electrode.

13. (Withdrawn): The method of claim 6, wherein the pixel electrode comprises IZO.

14. (Withdrawn): The method of claim 6, wherein the data line and the semiconductor layer is formed using a single photoresist film.

15. (New): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

16. (New): The thin film transistor array panel of claim 15, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

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17. (New): The thin film transistor array panel of claim 15, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

18. (New): The thin film transistor array panel of claim 15, wherein the pixel electrode comprises IZO.

19. (New): The thin film transistor array panel of claim 15, wherein the passivation layer has second and third contact holes exposing end portions of the gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

20. (New): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole, wherein a bottom of the contact hole is formed by a portion of an upper surface of the drain electrode and a portion of an upper surface of the passivation layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

21. (New): The thin film transistor array panel of claim 20, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

22. (New): The thin film transistor array panel of claim 20, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

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23. (New): The thin film transistor array panel of claim 20, wherein the pixel electrode comprises IZO.

24. (New): The thin film transistor array panel of claim 20, wherein the passivation layer has second and third contact holes exposing end portions of the gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

25. (New): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the pixel electrode contacts an upper surface of the gate insulating layer.

26. (New): The thin film transistor array panel of claim 25, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

27. (New): The thin film transistor array panel of claim 25, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

28. (New): The thin film transistor array panel of claim 25, wherein the pixel electrode comprises IZO.

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29. (New): The thin film transistor array panel of claim 25, wherein the passivation layer has second and third contact holes exposing end portions of the gate line and the data

line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

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